Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently Amended) A method for predicting delay of a multi-million gate sub-micron ASIC design, the method comprising the steps of:

(a) automatically partitioning a netlist into at least two timing-independent logic cones such that a timing effect of a first logic cone does not propagate to, or affect, a second logic cone in the design; and

(b) running respective instances of a delay prediction application on the timing-independent logic cones on at least two computers in parallel.

2. (Cancelled)

3. (Currently Amended) The method of claim 1 wherein partitioning the netlist includes ~~2 wherein step (a) (i) further includes the step of:~~

~~(ii)~~ partitioning the netlist into one global cone and multiple design cones.

4. (Original) The method of claim 3 further including the step of:

(c) merging output from the instances of the delay prediction application into a final output file.

5. (Original) The method of claim 4 further including step of using a partitioning program to automatically partition the netlist.

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6. (Original) The method of claim 5 further including step of: running the global clock cone through a monolithic delay prediction application.

7. (Original) The method of claim 6 further including step of: inputting output from the monolithic delay prediction application and the design cones into the respective instances of delay prediction applications.

8. (Original) A method for predicting delay of a multi-million gate ASIC design, the method comprising the steps of:

(a) partitioning a netlist into timing-independent cones including a global clock cone and multiple design cones;

(b) performing delay calculation on the global clock cone;

(c) performing delay calculation on the multiple design cones in parallel using as input the delay calculation output of the global clock cone; and

(d) merging results from the parallel delay calculations and the global delay calculation into an output file.

9. (Original) The method of claim 8 whercin step (a) further includes the step of:

(i) partitioning the netlist so that each of the multiple design cones includes approximately a same number of gates.

10. (Original) The method of claim 9 wherein step (b) further includes the step of:

(i) forming the global clock cone by identifying clock networks, reset pins, and logic controlled by a clock throughout the ASIC design.

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11. (Original) The method of claim 10 wherein step (b) further includes the step of:

(ii) calculating delays for the global clock cone using a monolithic delay prediction application.

12. (Original) The method of claim 11 wherein step (c) further includes the step of:

(i) using a global delay output file and the design cones as input to parallel delay prediction applications.

13. (Original) The method of claim 12 wherein step (c) further includes the step of:

(ii) allocating one computer to run one instance of the delay prediction application, and using each delay prediction application to perform delay calculations on one design cone.

14. (Original) The method of claim 13 wherein step (c) further includes the step of:

(iii) starting the delay prediction applications on each computer at the same time and running the applications in parallel so that delay output files for each cone are produced at approximately the same time.

15. (Original) The method of claim 14 wherein step (d) further includes the step of: using scripts to merge the global delay output file and the delay output files into a final output file.

16. (Original) A method for partitioning a netlist into timing-independent blocks of logic for distributed delay prediction, the method comprising the steps of:

(a) initializing all data structures related to cone traversal;

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(b) finding a global clock cone;

(c) finding normal design cones;

(d) merging the design cones if a number of design cones found is more than a number of computers available to perform the distributed delay prediction;

(e) creating a clock network;

(f) transforming the global clock cone into a writer cone and a write netlist;

(g) transforming the normal design cones into writer cones; and

(h) generating for each cone a netlist, a prospective pin list file, and a force ramptime pin list file.

17. (Original) The method of claim 16 further including step of:

(i) providing each netlist that was generated for each cone to one of the available computers, such that all of the available computers perform the delay prediction on the netlists in parallel.

18. (Original) The method of claim 17 wherein step (e) further includes the step of: creating the clock network using multithreading.

19. (Original) The method of claim 18 wherein step (g) further includes the step of: transforming the normal design cones using multithreading.

20. (New) The method of claim 4, wherein merging output from the instances of the delay prediction application into a final output file includes merging each output into a standard delay format (SDF) output file.

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